### Jointly Organized by Electronics & ICT Academies



IITR, MNITJ, NITP, IIITDMJ, IITG http://www.mnit.ac.in/eict

### Chairman, EICT Academy & Director MNIT Jaipur Prof. Narayana Prasad Padhy

Chief Investigator, EICT Academy Prof. Vineet Sahula, ECE

**Coordinator,** EICT Academy Dr. Satyasai Jagannath Nanda, ECE

**Co- Chief Investigators**, EICT Academy Prof. Lava Bhargava, ECE Prof. Pilli Emmanuel Shubhakar, CSE Dr. Ravi Kumar Maddila, ECE

Objective (Electronics & ICT Academy-Phase II)

1)To conduct specialized FDPs for faculty/mentor training in line with the vision of MeitY by promoting emerging areas of technology and other high-priority areas that are pillars of both the "Make in India" and the "Digital India" programs.

2) To promote synergy and collaboration with industry, academia, universities and other institutions of learning, especially in emerging technology areas.

3) To support the National Policy on Electronics 2019 (NPE 2019) which envisions positioning India as a global hub for ESDM sector, including MeitY Schemes/policies such as Programme for Semiconductors and Display Fab Ecosystem; India Al; National Programme on Al, Production Linked Incentive Scheme for IT Hardware & Large-Scale Electronics Manufacturing; EMC; SPECS; Chips to System (C2S); etc.

4) To promote standardization of FDPs through Joint Faculty Development Programmes.

5) To support the vision of the National Education Policy (NEP 2020), which mandates that Indian educators go through at least 50 hours in professional development programmes per year.

6) To design, develop & deliver specialised FDPs on emerging technologies/ niche areas/ specialised modules for specific research areas for Faculty in Higher Education Institutions (HEI), besides FDPs on multidisciplinary areas connected with ICT tools and technologies and other digital hybrid domains, covering a wide spectrum of engineering and non-engineering colleges, polytechnics, ITIs, and PGT educators.

# **Online Programme**

Intricacies of Analog & Mixed Signal design

### Faculty Development Programme Electronics & ICT Academy under aegis of



# 17th - 28th Feb 2025

meity.gov.in/content/schemes-projects

An intensive 40 Hours Training Programme in online mode is being organized for faculty and doctoral students of engineering and technological institutions. It is also open to working professionals from industry/organizations. The main theme of training program will be oriented around exploring the state of the art methods for Intricacies of Analog & Mixed Signal design. The programme will be run during **4** -8 PM <u>daily</u>.

## Experts/Speakers-

- 1) Prof. Sreehari rao patri, NITW, Prof Gjendranadh, IITH
- 2) Prof Saurabh Saxena, IIT Madras, (consent awiaited),
- 3) Prof Kapil Jainwal, IITH, ,IDr Chitra

4) IIT Kanpur (consent awaited) Prof Nagendra IITM (consent awaited)

### **Programme Modules:**

Basic MOS Device Physics Amplifiers- differential amplifiers, frequency response of amplifiers- common source/gate, Cascode, CMRR, Gilbert cell, Miller effect

**Noise** in amplifiers, current mirrors,

OpAmp- multistage, OTA, stability & frequency compensation

**Sample and Hold Circuits:** Basic S/H circuit, effect of charge injection, compensating for charge injection, bias dependency, bias independent S/H

**D/A Converter**: – General considerations, Static non-idealities and Dynamic non-idealities; Current-steering DAC – Binary weighted DAC, Thermometer DAC, Design issues, Effect of Mismatches.

**A/D converter**: – General considerations, static and dynamic non-idealities. Flash ADC – Basic architecture, Design issues,, Effect of non-idealities Interpolative and Folding architectures. Successive Approximation ADC; Pipeline ADC. Over sampling ADC – Noise shaping, Sigma-Delta modulator.

**PLLs:** Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Liberalized Small-Signal Analysis, Second-Order PLL Model, Limitations of the Second-Order Small-Signal Model, PLL Design Example

### Joint-Principal Coordinator (MNIT Jaipur):

Dr. Menka Yadav <u>fdp.academy@mnit.ac.in</u>

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### Registration:

Registration is open to faculty, working professionals, industry persons, doctoral, postgraduate and graduate students. Participants will be admitted on first-come first-served basis. Register online at-

http://online.mnit.ac.in/eict/

Certification Fee: Academic (faculty/Students): Rs. 500/-

- Working professionals, Industry/Others: 1500/-
- (A) Fee once paid will not be refunded back.

(B) The fee covers online participation in the programme, tutorial notes and examination, certification charges.

(C) The organizers should receive the registration amount through online mode-NEFT/UPI, provided at the registration portal.

(D) Detailed schedule will be shared after receiving registration form.

→ For any other query, email us at <a href="mailto:fdp.academy@mnit.ac.in">fdp.academy@mnit.ac.in</a>, <a href="mailto:academy@mnit.ac.in">academy@mnit.ac.in</a>, <a href="mailto:academy@mnit.ac.in">academy@mnit.ac.in</a>)

**MNIT Jaipur** one of the oldest NITs, the institute has a rich heritage of sixty years producing world class engineers, managers, architects and scientists. Ranked 43rd nationally in the NIRF ranking-2024 (Engineering), the institute offers learning opportunities for undergraduate, postgraduate students, and researchers in various domains. Having a lush green campus of over 317 acres within the heart of the pink city, close to Jaipur International Airport, the campus offers a safe and lively environment. A world class teaching infrastructure, state-of-art laboratories welcome you at the campus. The institute has a vision to impart education of international standards and conduct research at the cutting edge of technology.

